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SF-7141

B. E. - III (Sem. VI) (I.T.) Examination

May / June - 2011

Computer Architecture & Peripherals

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. - 3 (SEM. 6) (I.T.)

Name of the Subject :

☛ COMPUTER ARCHITECTURE & PERIPHERALS

☛ Subject Code No. : 7 1 4 1 ☛ Section No. (1, 2,.....) : NIL

Seat No. :

Student's Signature

(2) Figures to extreme right indicate maximum marks.

(3) Make necessary assumptions, if required.

1 (a) Answer the following : **10**

(i) Control memory register is present in _____.

(ii) "Instruction code is a container for opcode." State true or false.

(iii) Define Supervisor mode.

(iv) What is meant by effective address in addressing mode ?

(v) What is the need of IOP in computer system ?

(vi) Give the full form of SKI.

(vii) Which information is stored by status bit register ?

(viii) State the main objective of DMA.

(ix) Enlist the components of CPU.

(x) What is the difference between microprogram and microinstruction ?

(b) Draw the diagram for common bus system. **5**

(c) Give the difference between : **5**

(i) Hardwired control and microprogrammed control.

(ii) Register stack and memory stack

2 (a) Attempt any two : 12

(i) Discuss the following memory reference instructions with microoperations :
(a) ISZ
(b) BSA
(c) STA

(ii) Convert the following expressions into postfix notation.
(a) (A + B) * C-D / (E ^ F + G)
(b) (A – B / C) + D * E / (F * G ^ H)

(iii) Explain the following terms with respect to microprogrammed control organization.
(a) Control memory
(b) Pipeline register
(c) Sequence

(b) What is the difference between a direct address and an indirect address instruction ? Support your answer with neat sketches. 3

3 (a) Explain the interrupt cycle with its flowchart. 8

(b) Write a program to evaluate the following arithmetic statement using a general purpose computer with three address instructions and stack organized computer with zero address instructions : 7
X = (A + B / C) * D + E - F

OR

3 (a) The memory unit of a computer has 512K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of seven addressing modes, a register address field to specify one of 63 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the instruction is in one memory word. 8

(b) Discuss general register organization with neat sketches. 7

4 (a) Answer the following : **10**

(i) What is the purpose of parallel processing in computer system ?

(ii) What is non-restoring method for binary division ?

(iii) Define : address space.

(iv) What is Baud-rate ?

(v) In which floating point operations alignment of mantissas is not required ?

(vi) "When a word is written in a Content Addressable Memory (CAM), no address is given." State true or false.

(vii) What is biased exponent ?

(viii) A special very-high-speed and small memory called _____ memory.

(a) Main
(b) cache
(c) auxiliary
(d) associative

(ix) What is meant by Vector processing ?

(x) Explain locality of reference in brief.

(b) Give the Flynn's classification and explain the same. **6**

(c) Explain the memory hierarchy with neat sketches in brief. **4**

5 (a) Attempt any two : **12**

(i) Explain associative memory its match logic.

(ii) Discuss pipeline conflicts in detail.

(iii) Discuss Cache coherence problem with its proposed solution(s).

(b) Explain overflow situation in binary addition with example. **3**

6	(a)	Discuss Booth Multiplication algorithm in detail with example.	8
	(b)	Explain four segment pipeline in detail.	**7**

OR

6	(a)	List and explain the mechanism for handling of branch instructions.	8
	(b)	Explain the types of mapping procedures when considering the organization of cache memory.	**7**